

ELEN E3106/4106 Lecture 21

MOSFETs Part I

Outline

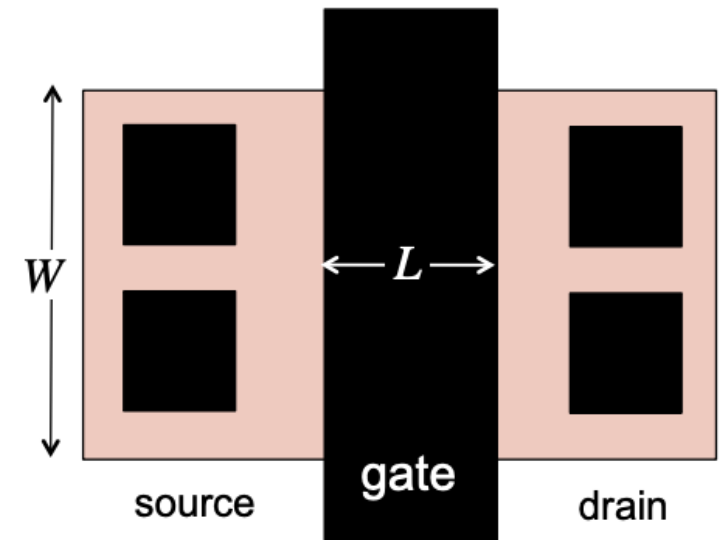
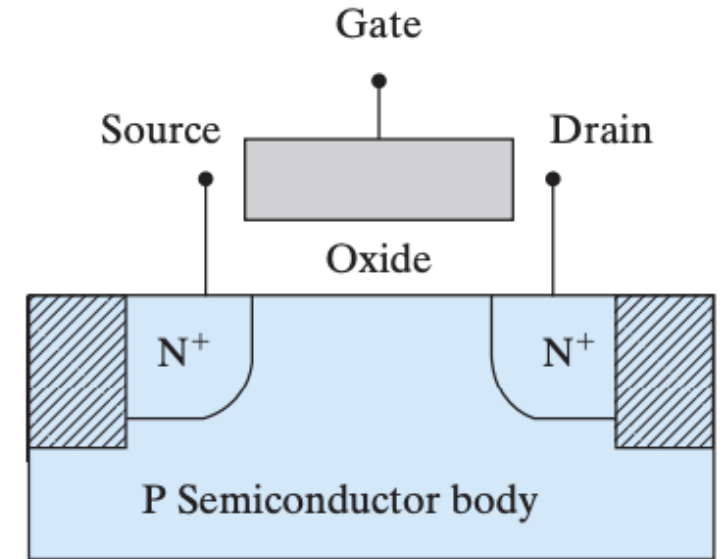
- MOSFET structure
- MOSFET as a switch
- Regions of operation
- Output and transfer characteristics
- CMOS device and circuit technology

Assignments:

Homework 8 due Monday, December 1st by 11:59pm

Basic Device Structure

- **Metal Oxide Semiconductor** _____
- Most prevalent semiconductor device in ICs!
- Essentially, a MOS capacitor with carrier wells on either side. This means we have 2 _____!
- 3 terminal device
- What is a field-effect transistor (FET)?
 - The _____ on one terminal (_____) creates an E-field through the oxide that either allows or prevents conduction (e.g. current) between the other two terminals (_____)
- Unipolar: only one type of charge carrier is significant to their operation unlike _____



Comparison with BJT and Nomenclature

1. Transistor Amplification: a small signal (I or V, terminal #2) can control a large signal (usually I, flowing between terminal #1 and #3)

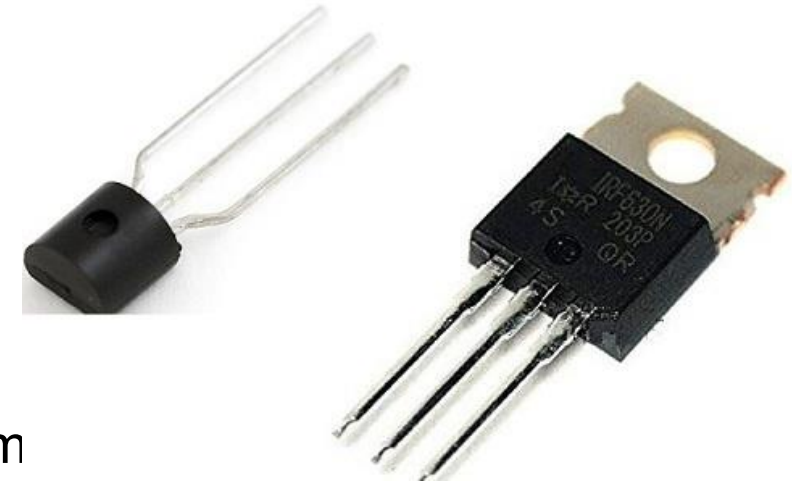
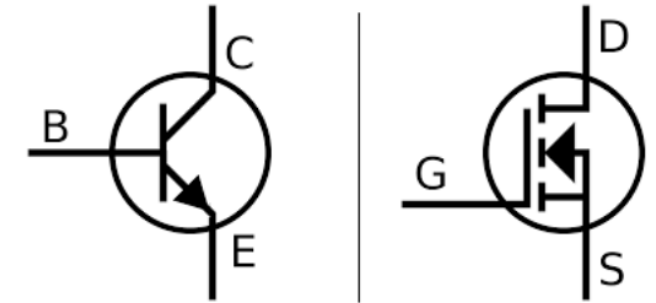
2. Transistor Switching: the transistor can be turned _____.

1) BJT: small input current (faucet) controls large output current (hose)
e.g. current-controlled current source

2) FET: small input voltage (faucet) controls large output current (hose)
e.g. _____

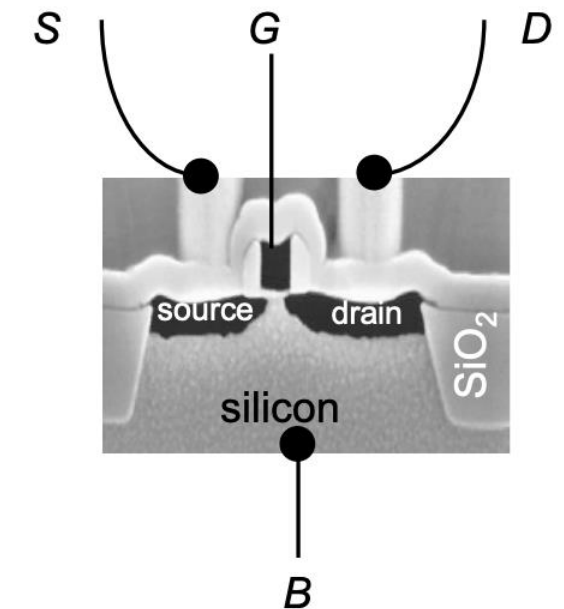
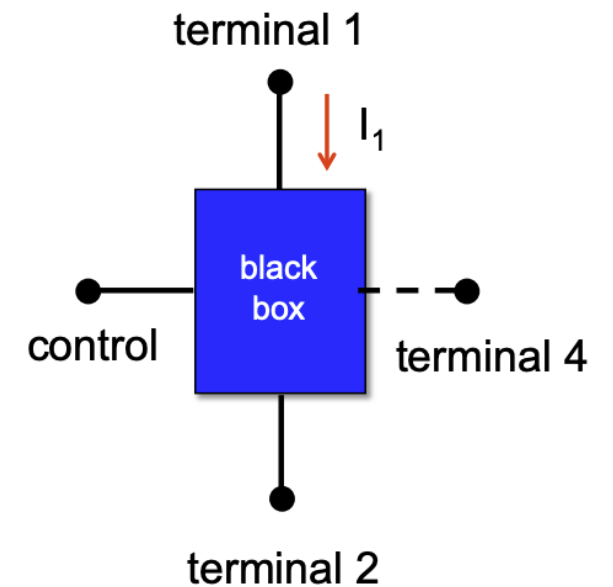
- Recall: A terminal is any externally available point of connection (_____, infinite carrier source/sink)
- How many terminals does a transistor **usually** have? _____
 - Terminal 1: brings current into the transistor.
 - BJT: Emitter = MOSFET: _____
 - Terminal 2: carries current out.
 - BJT: Collector = MOSFET: _____
 - Terminal 3: acts as a handle to control the current flow (input term)
 - BJT: Base = MOSFET: _____

BJT vs FET (Transistors)



Transistor as a “Black Box”

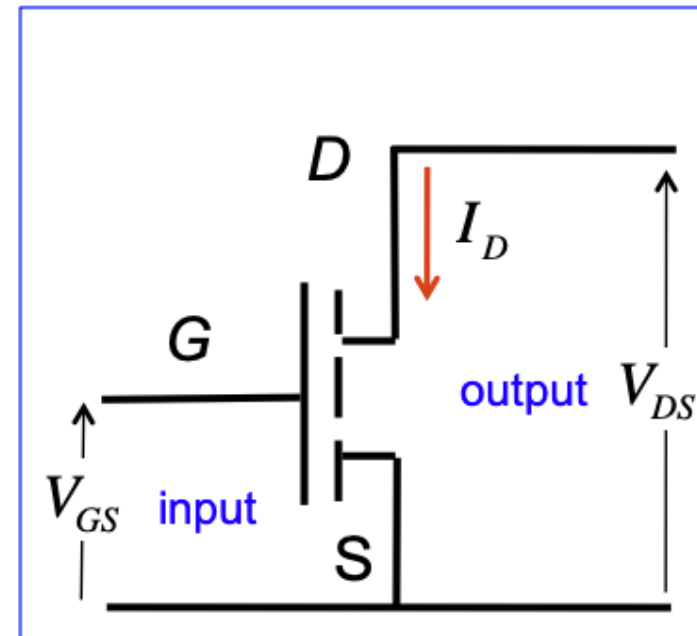
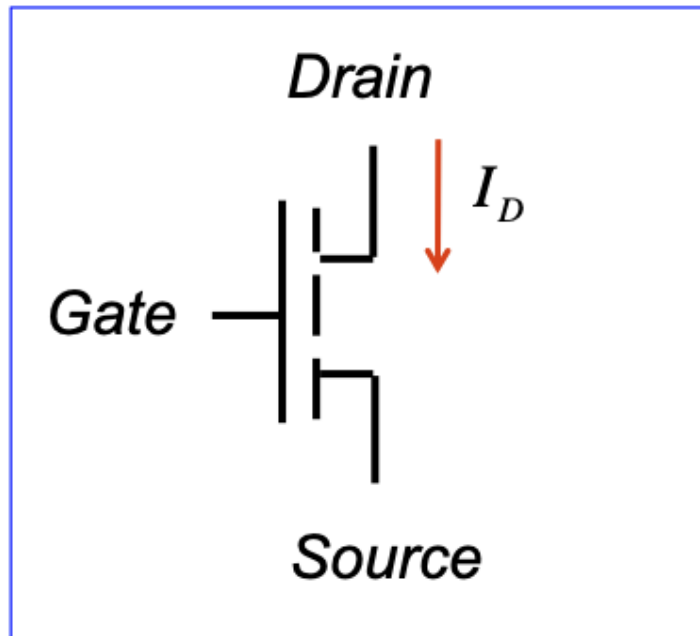
- A black box is any complicated electronic device like a _____ whose behavior can be observed entirely in terms of _____ even if the internal structure is not known
 - We have already looks at one example: _____
- There are many kinds of transistors!
 - MOSFETs
 - Schottky-barrier (SB) FET
 - High electron mobility transistor (HEMT)
 - FinFET
 - BJT
 - Heterojunction bipolar transistor
 - SpinFET, etc.
- What’s the 4th terminal for on the diagram on the right?
- The body is frequently connected to the _____ to ensure both p-n junctions at source/body and drain/body are not _____ to prevent large unwanted current flowing from body into source or drain



(Texas Instruments, ~ 2000).

MOSFET Circuit Symbol and Configuration

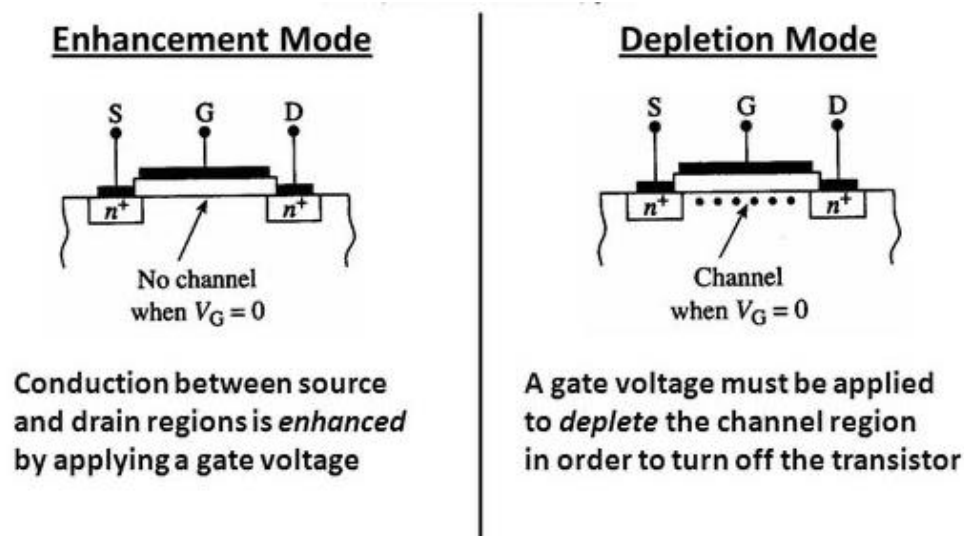
- Circuit symbol (left) and common source configuration (right). Source is often _____.
- We are interested in the $I - V$ characteristics in terms of the drain current ____, and various voltages
- $I_D - V_{GS}$ for fixed V_{DS} are called the *transfer characteristics*
- $I_D - V_{DS}$ for fixed V_{GS} are called the *output characteristics*



MOSFET Enhancement and Depletion Modes

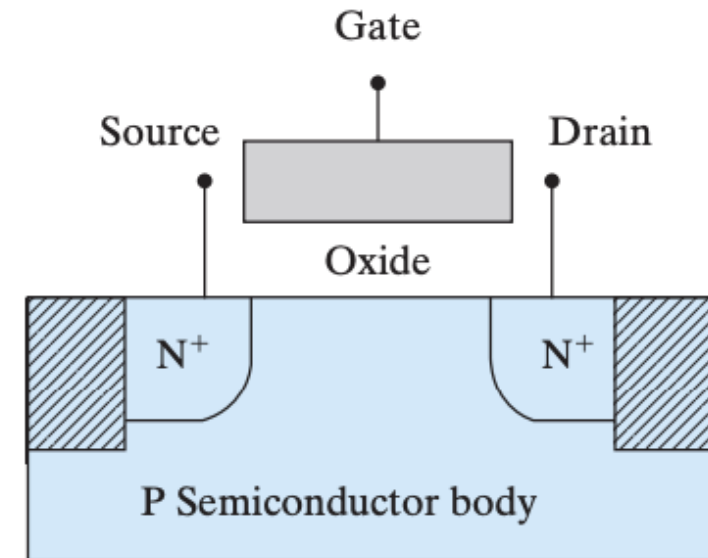
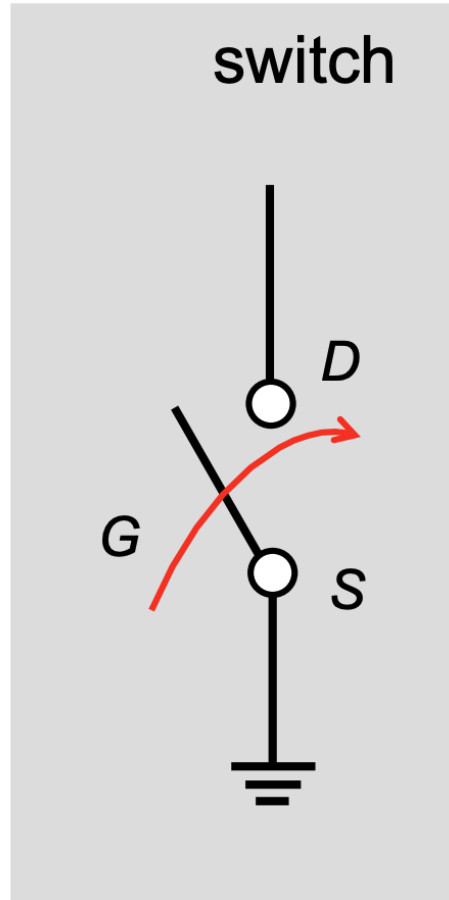
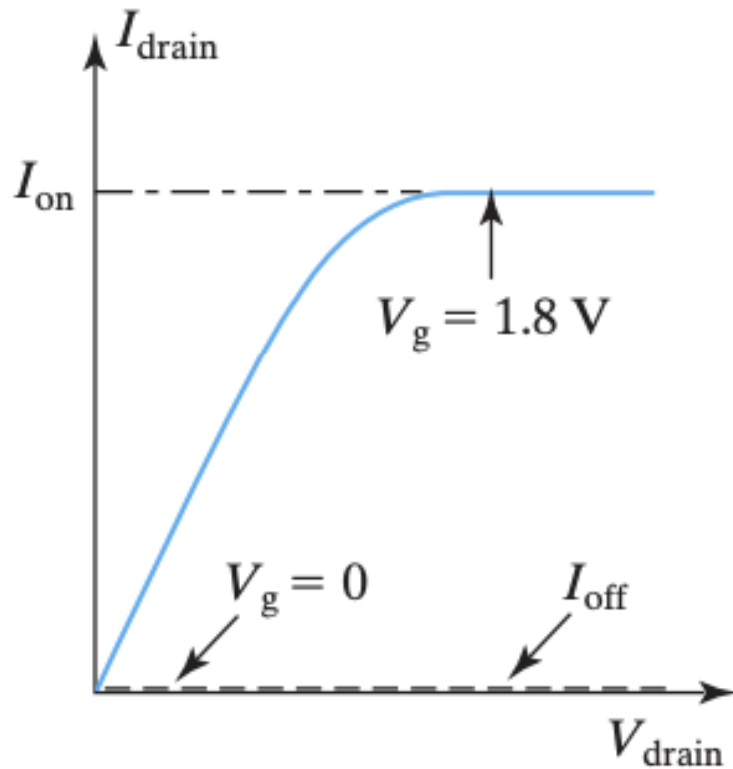
Two “modes” or types of transistors exist

1. Enhancement-mode (“_____”): The channel is devoid of carriers at $V_g = \text{_____}$ and $|V_g| > |V_{th}|$ is required to create the channel and turn it “on”
 2. Depletion-mode (“_____”): The channel is already present and conducts at $V_g = 0$ V. Device requires an _____ to turn it “off”
- Modern Si MOSFETs are all enhancement-mode for easier circuit design and better power efficiency, so we will be focusing on e-mode



MOSFET As a Switch

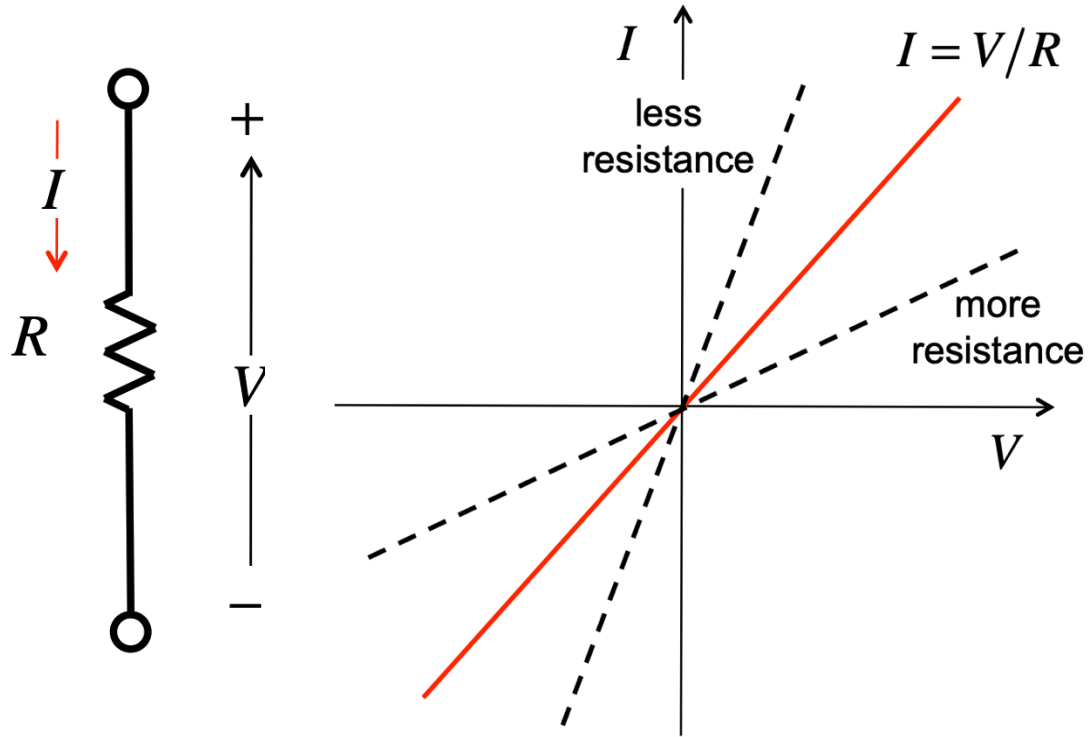
- At the basic level, we can think of the MOSFET as an on-off switch
- The gate voltage ____ determines whether current I_D flows between the source and drain



I-V Characteristics of Basic Two Terminal Components

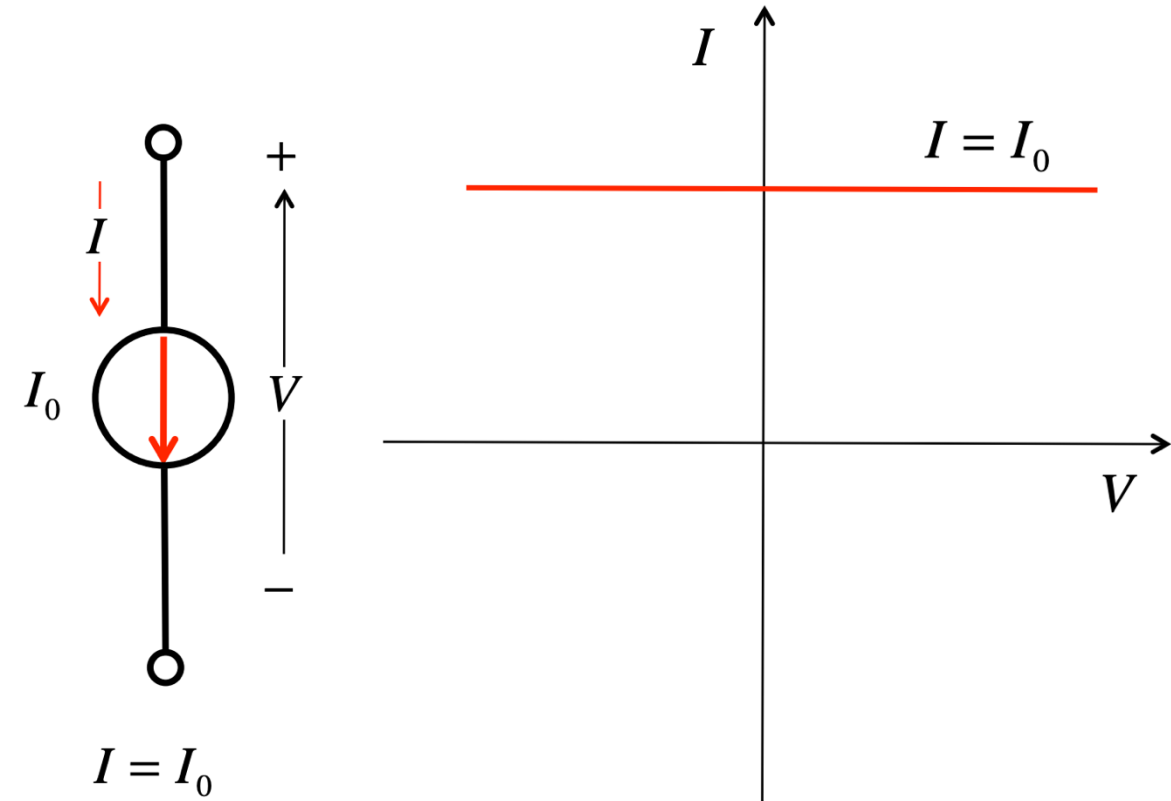
Resistor

Ohm's Law: $I = V/R$



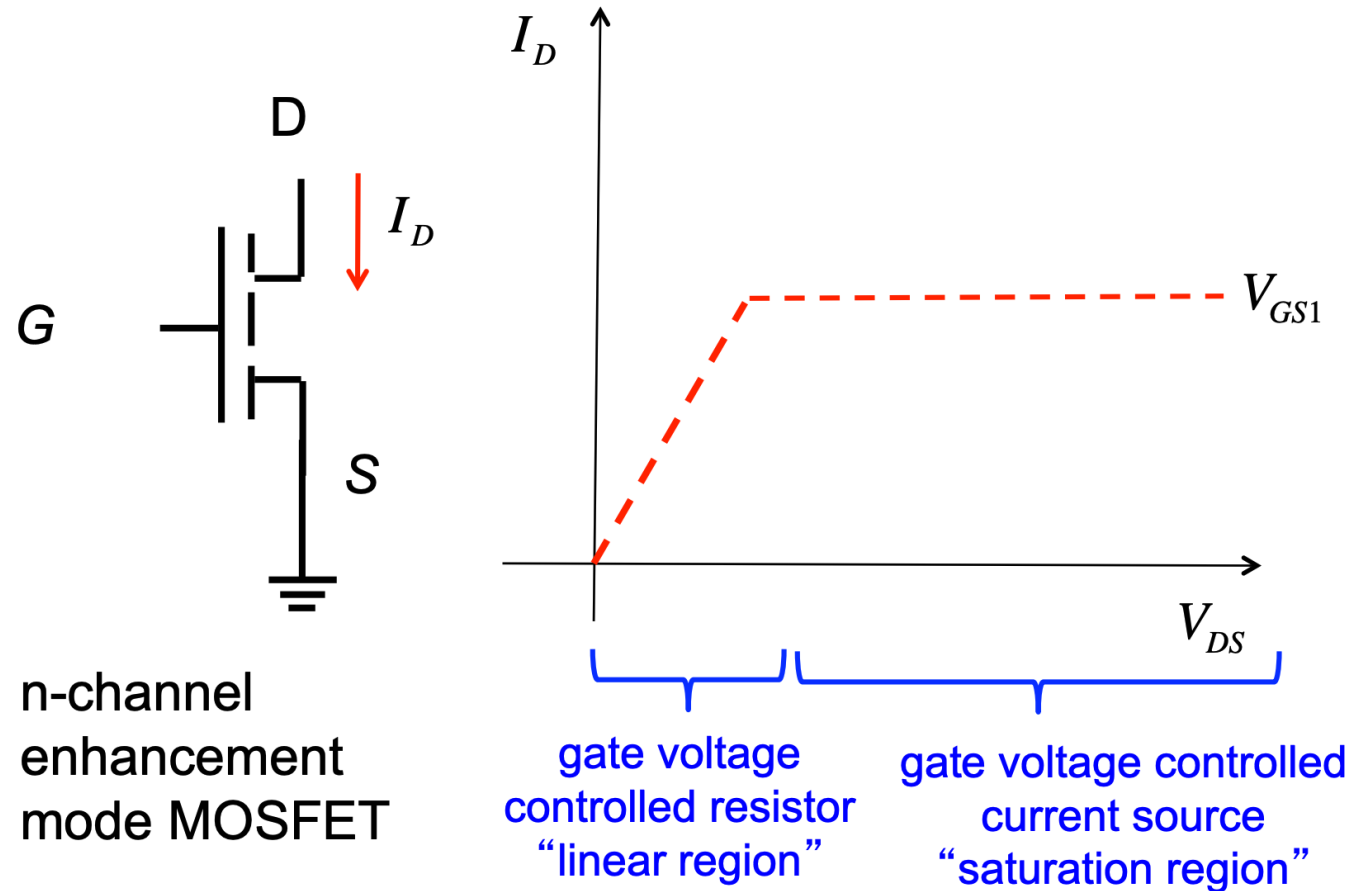
Ideal Current Source

Current flowing from source is constant regardless of the _____



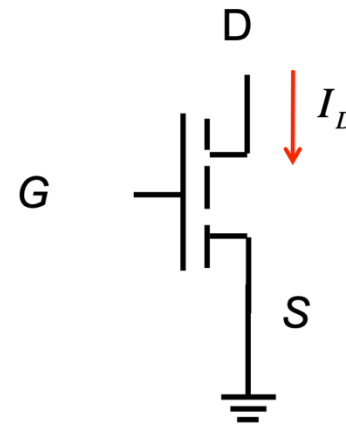
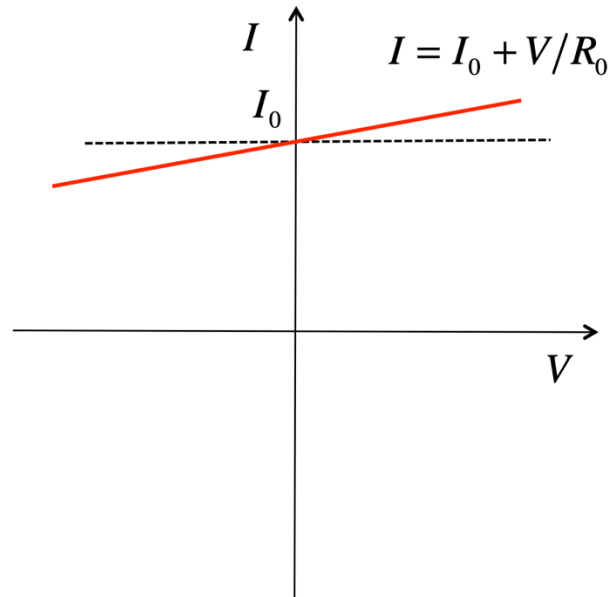
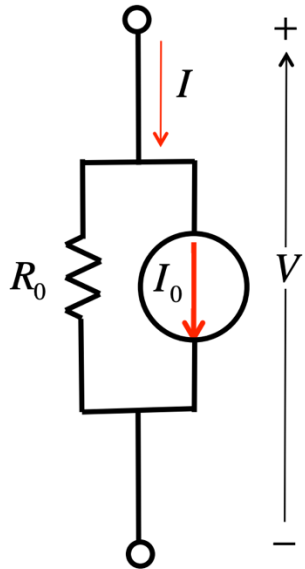
Ideal I-V Characteristics of a MOSFET

- At low voltages, the device operates as a _____
- At higher voltages, the device operates like a _____

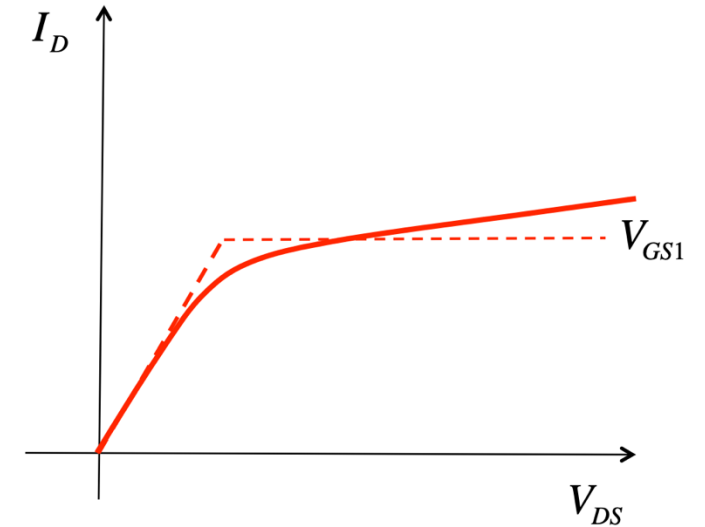


Realistic I-V Characteristics of a MOSFET

- Real (non-ideal) current sources have an internal source resistance, so the curve is not _____
- The MOSFET also exhibits this non-ideality



n-channel
enhancement
mode MOSFET

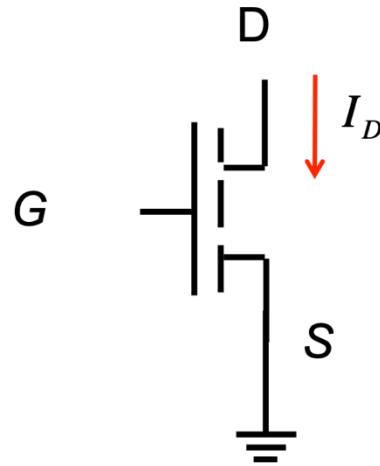


MOSFET Output Characteristics

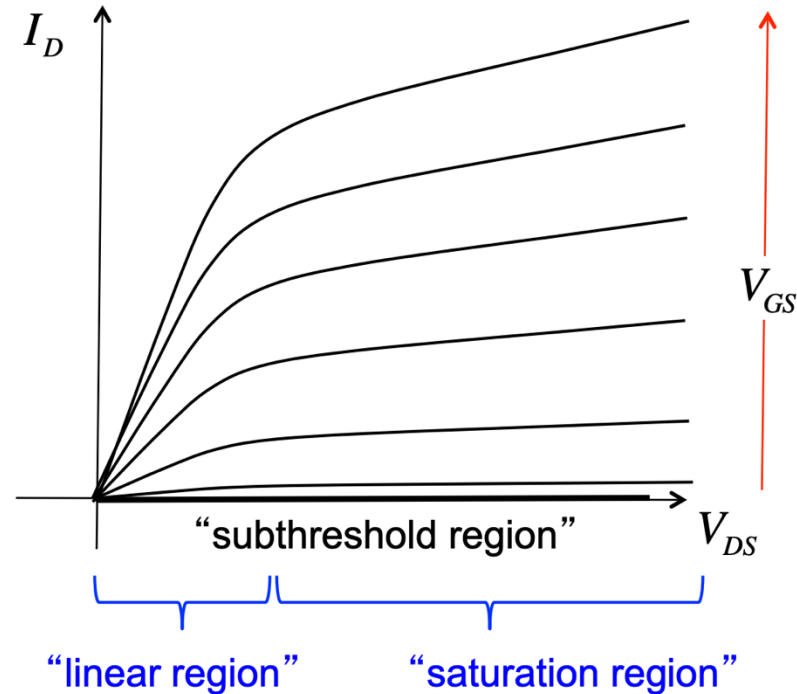
- $I_D - V_{DS}$ sweep where each curve is measured at a _____ V_{GS} value
- Note: Voltages can be denoted by one or two subscripts (e.g. ____ or ____). Including the “s” for source is essential in complex cases where the source is not necessarily _____. For our discussions, we will assume the source is grounded and _____ = _____

$$V_g = V_{\text{gate}} - V_{\text{ground}}$$

$$V_{gs} = V_g - V_s.$$

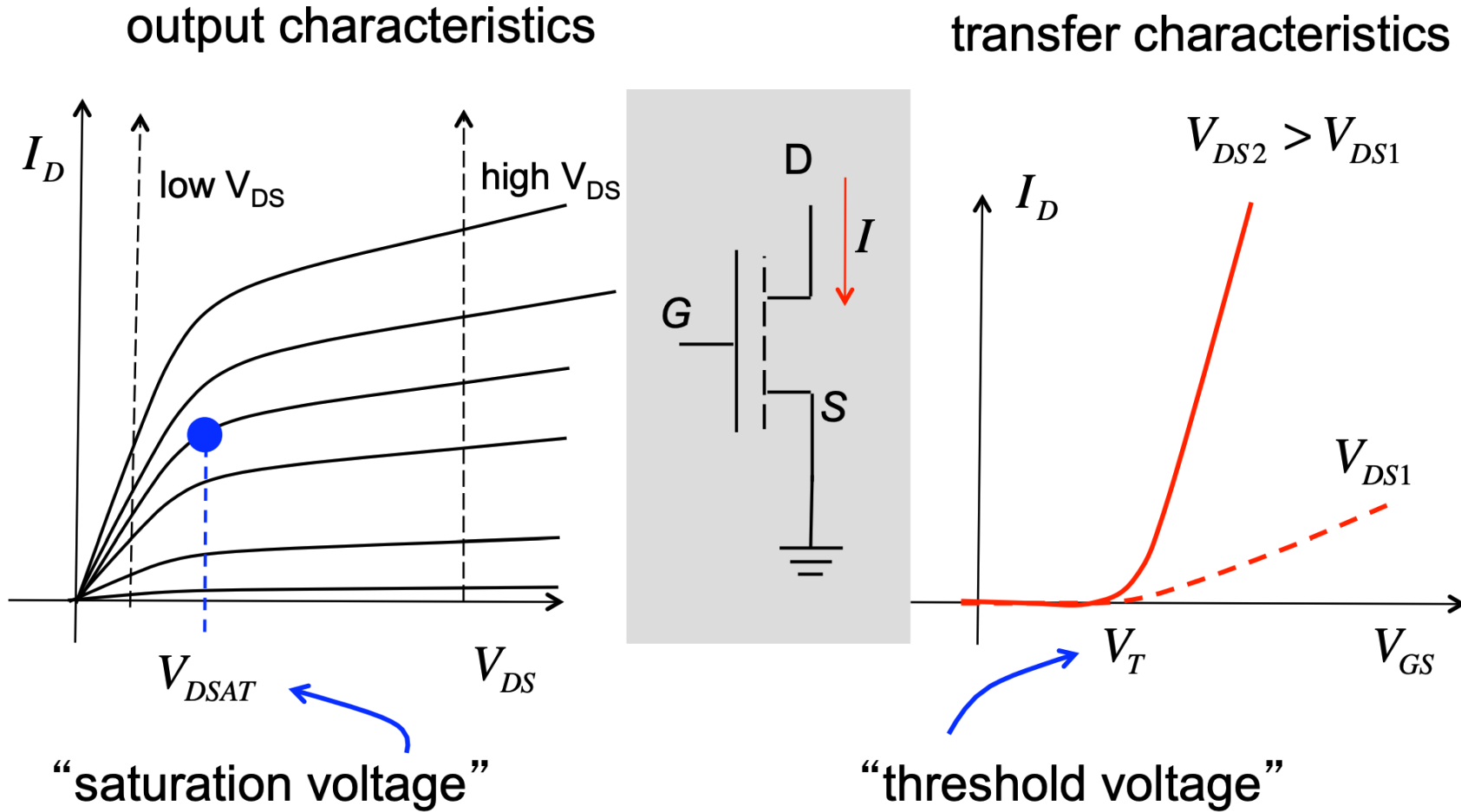


n-channel
enhancement
mode MOSFET



MOSFET Transfer Characteristics

- $I_D - V_{GS}$ sweep where each curve is measured at a fixed V_{DS} value



MOSFET Regions of Operation

1. Cut-off Region: $V_{GS} < V_t$, almost no current flow. Device is “off”, switch is _____, and the inversion channel is not present or has very low conductivity.
2. Linear (_____ or _____) Region: : $V_{GS} > V_t$ while $V_{DS} < V_{Dsat}$. The switch is “on” and behaves as a variable resistor (e.g. the resistance is controlled by V_{GS}).
3. Saturation: $V_{GS} > V_t$ while $V_{DS} > V_{Dsat}$ As a higher V_{GS} is applied, the current will reach its maximum and saturate, behaving as a current source controlled by _____).

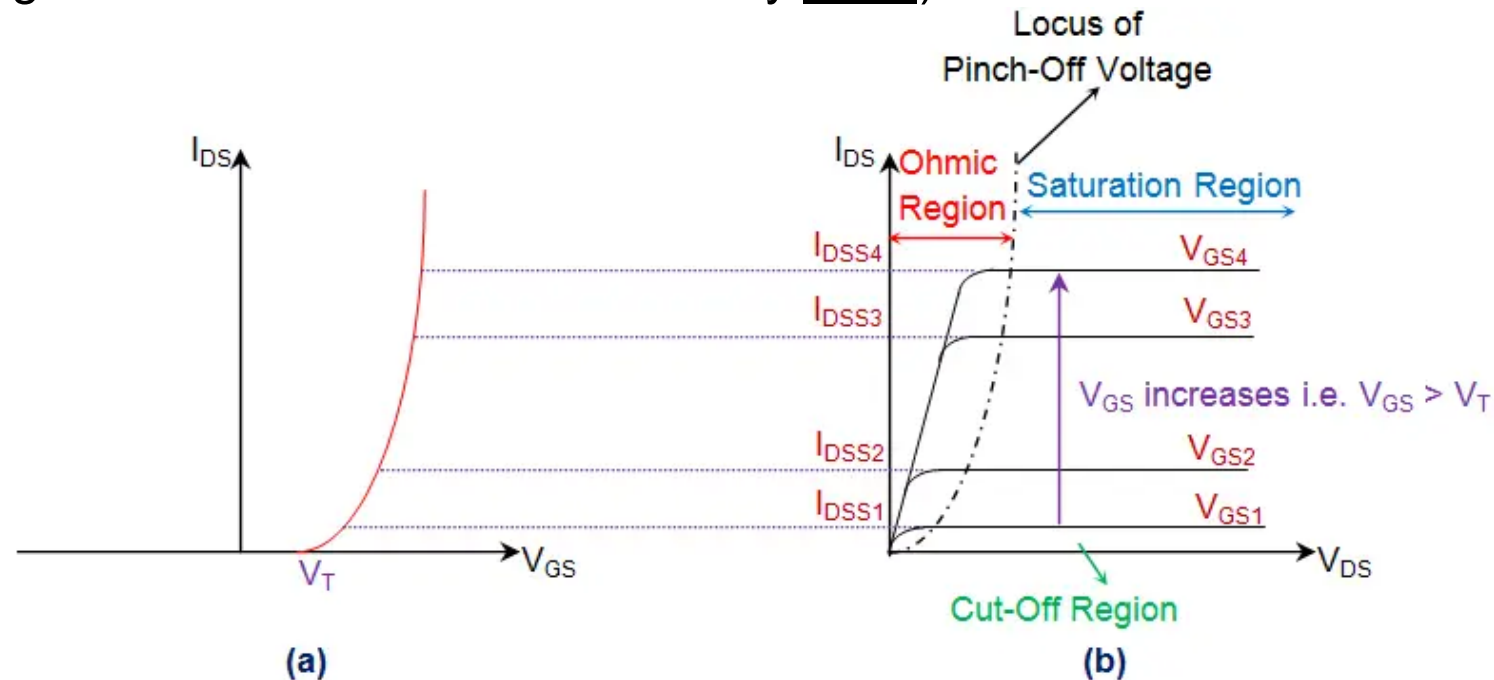
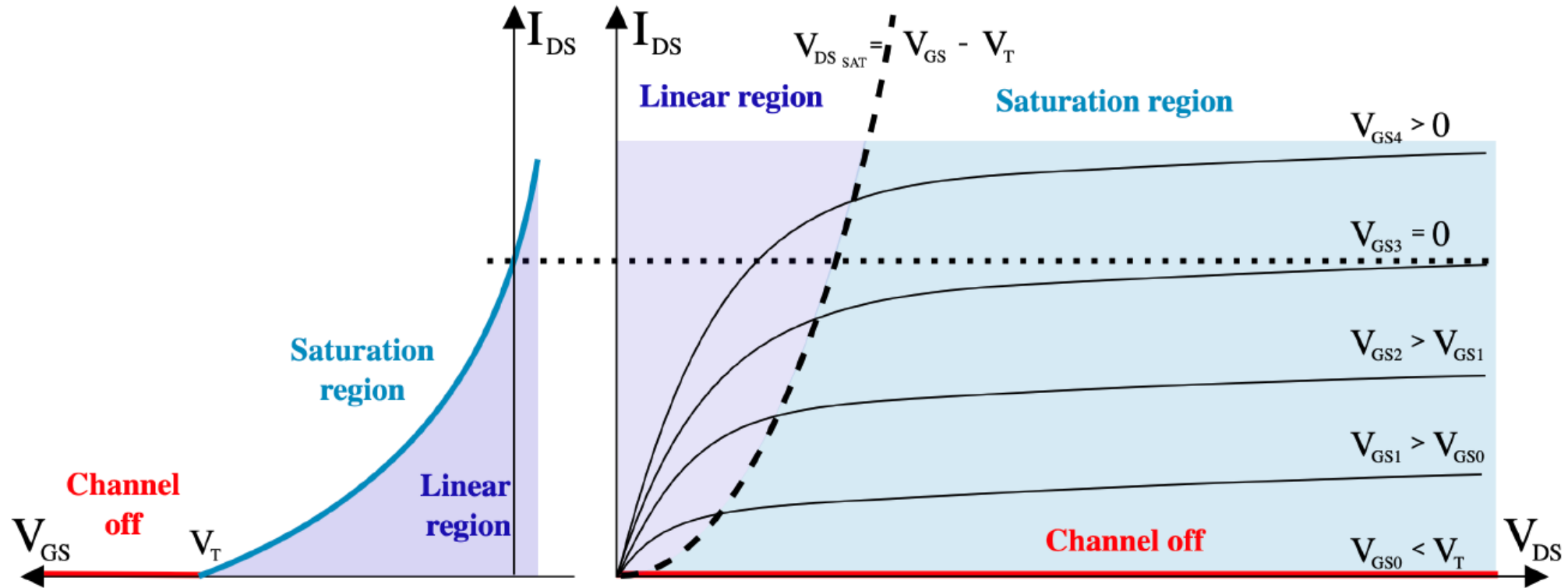


Figure 1 *n*-Channel Enhancement type MOSFET (a) Transfer Characteristics (b) Output Characteristics

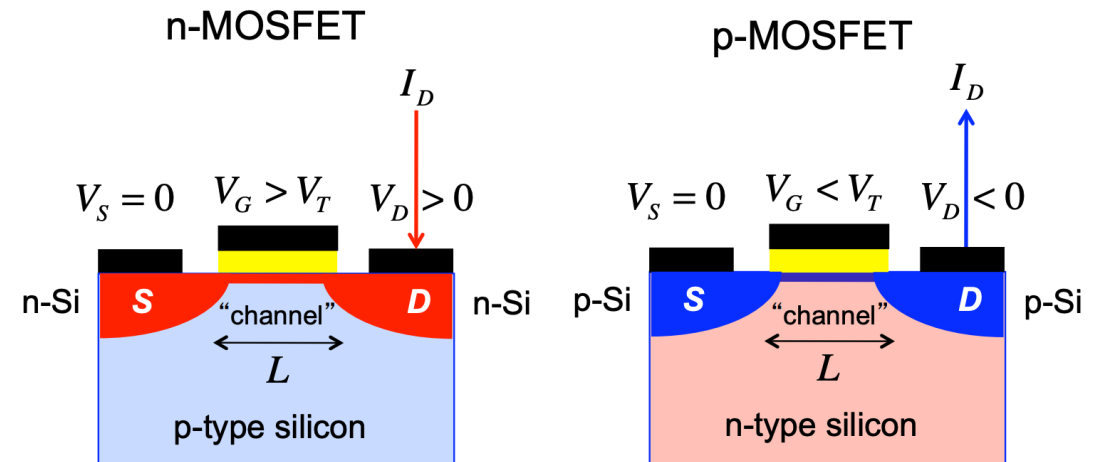
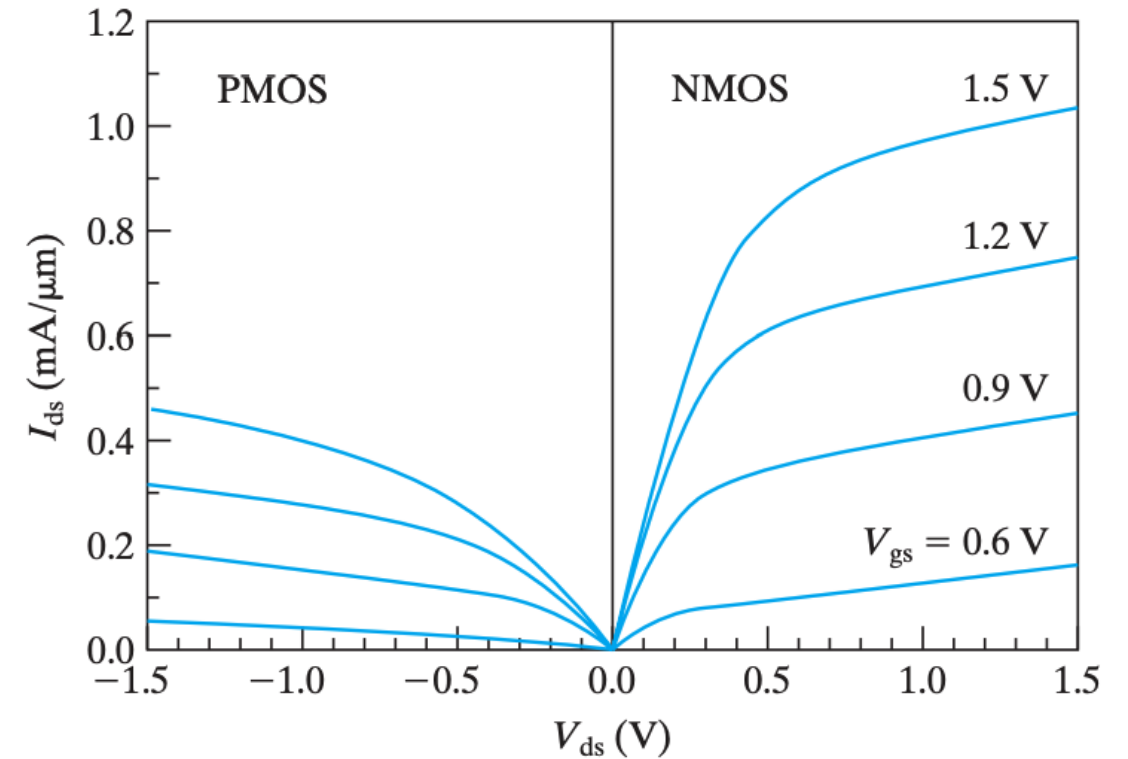
What about Depletion-Mode I-V?

- Depletion-mode FETs have a _____ V_{GS} because the channel is present without any applied bias ($V_{GS} = 0$ V)



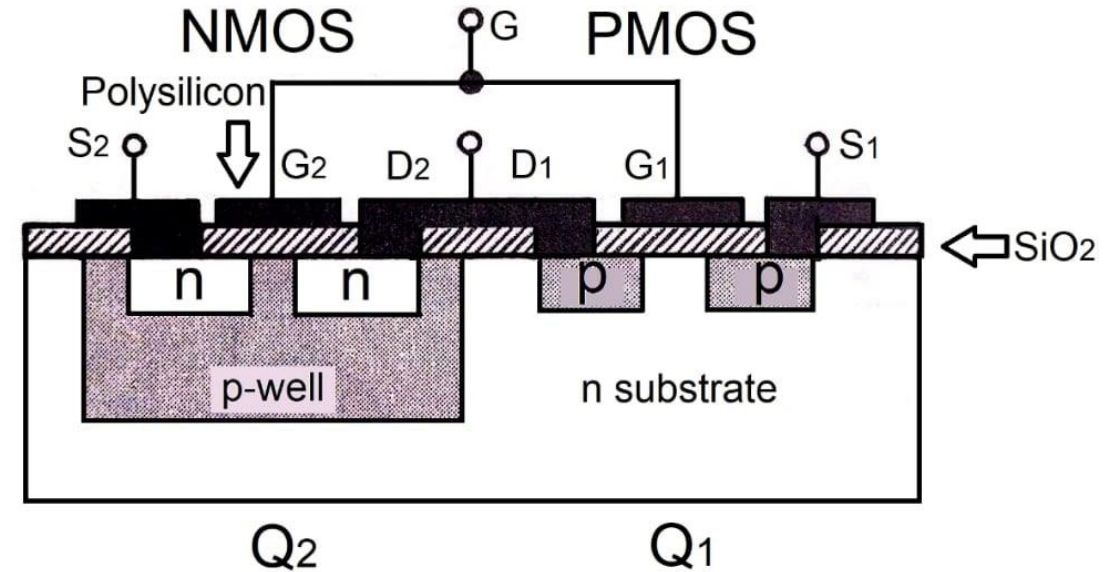
What about p-channel MOSFETs?

- The curves are qualitatively similar, but the current is about half as large in the p-channel MOSFET than the n-channel MOSFET. Why?
- The polarity of V_{DS} is reversed from that of n-channel MOSFET. Why?



CMOS Technology

- Complimentary MOS means the transistors operate in _____, p-type and n-type on the same chip
- The inversion layer is the conducting channel in a MOSFET.
- Like we learned with MOS capacitors....
 - N-MOSFET or NFET is an N-channel MOSFET
 - Inversion layer is _____ and the substrate is _____
 - P-MOSFET or PFET is a P-channel MOSFET
 - Inversion layer is _____ and the substrate is _____
- Primary application is high speed logic gates for digital circuits
- CMOS circuits have negligible DC input current, so the _____ is low because the “off” transistor limits the drain current to the leakage value
- Power dissipation is notable only during the input switching



CMOS Inverter Overview

- In binary arithmetic, logic functions are performed with _____

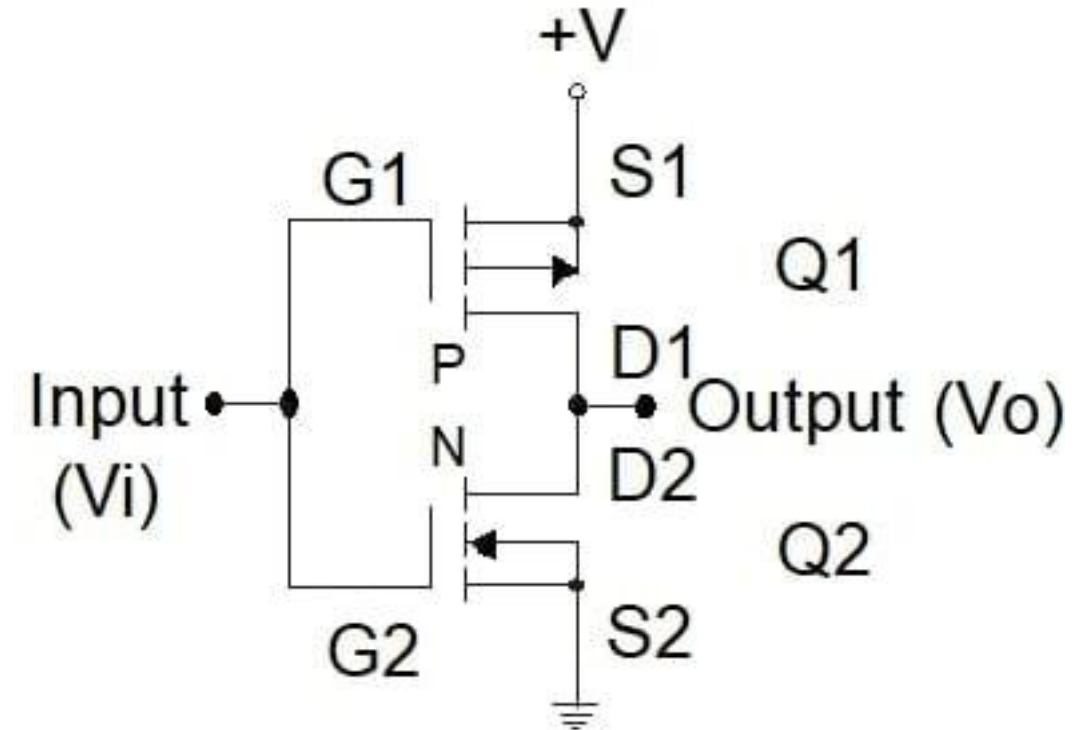
- Inverter is a logic element that reverses the logic input

- Truth table:

INPUT	OUTPUT
0	1
1	0

- We can build a PMOS or NMOS inverter, but the lowest power dissipation is achieved with CMOS
- Each transistor works as the load resistance of the other

Q1 is an E-mode PMOS
Q2 is an E-mode NMOS



Push-pull configuration:

- Gates are connected at the _____
- Drains are connected at the _____
- Sources are connected to the respective supply levels ($+V$ and ground)

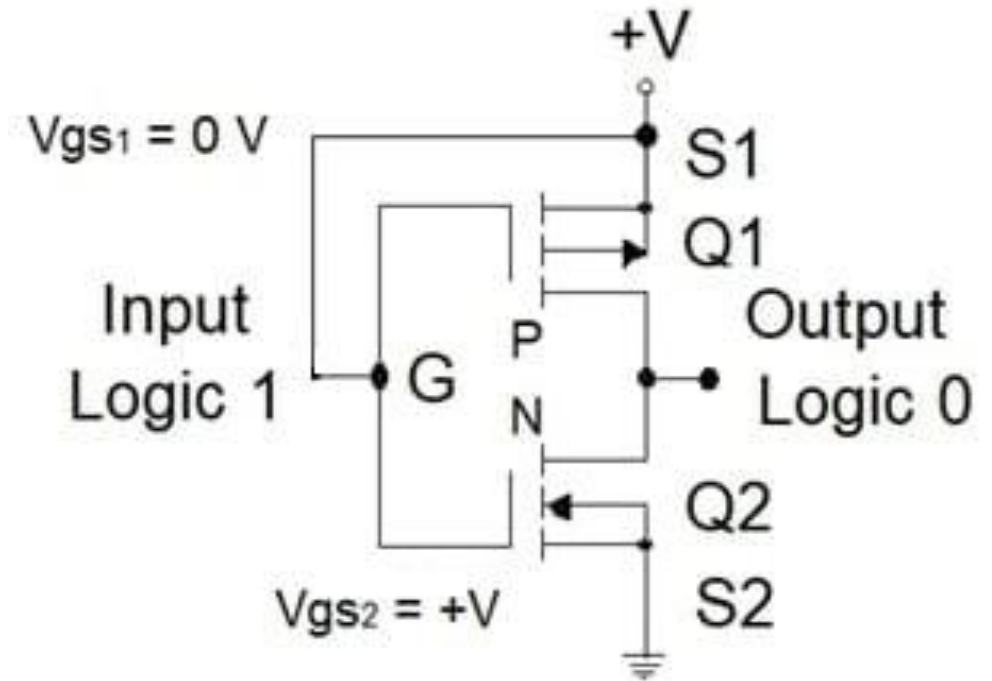
CMOS Inverter: Logic 1 to Logic 0

- What happens when we apply $+V_i$ to the gates? (Logic 1)
- V_{GS2} is (+), and Q2 is turned “on” with $R_{DS,Q2}$ very small
- But $V_{GS1} = 0$ since S1 is also at +V, so Q1 is kept “off” with very high $R_{DS,Q1}$
- The output voltage is computed using the voltage divider rule:

$$V_{out} = V_i \left(\frac{R_{DS,Q2}}{R_{DS,Q1} + R_{DS,Q2}} \right) \approx$$

- We have inverted the input Logic 1 to result in an output Logic 0

Q1 is an E-mode PMOS
Q2 is an E-mode NMOS



CMOS Inverter: Logic 0 to Logic 1

- Let's look at the opposite case where we connect V_i on the gates to ground (Logic 0)
- $V_{GS2} = 0$, and Q2 is kept “off” with $R_{DS,Q2}$ very high
- Now, $V_{GS1} = -V$ in Q1, and it is “on” with very low $R_{DS,Q1}$
- Once again, we use the voltage divider rule:

$$V_{out} = V_i \left(\frac{R_{DS,Q2}}{R_{DS,Q1} + R_{DS,Q2}} \right) \approx$$

- Thus, we have inverted the input Logic 0 to result in an output Logic 1
- NMOS “pulls-down” output to ground (0) while PMOS “pulls-up” output to $+V$ (1) when “on”

Q1 is an E-mode PMOS
Q2 is an E-mode NMOS

